THAT WHICH IS CLAIMED IS:

1. A power down circuit for use in a System on Chip SOC, comprising:

a plurality of circuit blocks (112, 412, 114, 414) in said SOC, each of said circuit blocks having a local clock (310);

a system clock (130) coupled to one or more of said circuit blocks (112, 412, 114, 414) and structured to act as said local clock (310) of selected ones of said plurality of circuit blocks;

a power control manager coupled to said plurality of circuit blocks (112, 412, 114, 414) and structured to provide a signal at least partially determining whether said system clock (130) will act as said local clock (310) of said plurality of circuit blocks; characterized in that one or more of the circuit blocks (112, 412, 114, 414) contain a shutdown circuit (300) structured to selectively prevent the system clock (130) from acting as said local clock (310) in said one or more of the circuit blocks after said shutdown circuit (300) receives a signal to shutdown (142) from said power control manager (140) and after said one or more of the circuit blocks have shutdown.

2. A power down circuit for use in the System on Chip SOC according to Claim 1, further characterized in that said shutdown circuit (300) is a clock separation circuit coupled to the power control manager (140) and structured to prevent said system clock (130) from acting as said local clock (310) in those said one or more of the circuit blocks that have

received said shutdown signal (142) and have completed any necessary tasks.

3. A power down circuit for use in the System on Chip SOC according to Claim 1, further characterized in that the power control module (140) is coupled to said shutdown circuit (300) through a request line (142) and through an acknowledgment line (144).

4. A power down circuit for use in the System on Chip SOC according to Claim 3, further characterized in that said clock separation circuit (300) includes a logic circuit (306, 308) coupled to said request line (142), said acknowledgment line (144), and said system clock (130), and said logic circuit is structured to generate said local clock (310) at the output of said logic circuit (306, 308) responsive to signals on said request line (142), said acknowledgment line (144), and said system clock (130).

5. A power down circuit for use in the System on Chip SOC according to Claim 1, further characterized in that said power control module (440) comprises a first register (446) coupled to a request line (142) of each of said circuit blocks (112, 114, 412, 414) and a second register (448) coupled to an acknowledgment line (144) of each of said circuit blocks (112, 114, 412, 414), and in that said first register (446) stores a datum indicating a state of each of the request lines (142) coupled to it, and in that said second register (448) stores a datum

indicating a state of each of the acknowledgment lines (144) coupled to it.

6. A power down circuit for use in the System on Chip SOC according to Claim 5, characterized in that it further comprises a CPU coupled to said power control module (140) that is able to determine states of said circuit blocks (112, 114, 412, 414) by querying said first register (446) and said second register (448).

7. A power down circuit for use in the System on Chip SOC according to Claim 1, characterized in that more than one system clocks are present in said System on Chip and are respectively structured to act as said local clock (310) of selected ones of said plurality of circuit blocks.

8. A method of powering down individual circuit blocks of a plurality of circuit blocks within a System on Chip, comprising the steps of:

generating a system clock signal (130) that is coupled to said plurality of circuit blocks (112, 114, 412, 414) and used as a local clock (310) for said plurality of circuit blocks;

generating a signal to power down (142) selected of the plurality of circuit blocks;

transmitting said signal to power down (142) said selected circuit blocks to a power down circuit (300); characterized in that the method further comprises:

accepting said signal to power down (142) at said power down circuit (300) in each of said selected circuit blocks (112, 114, 412, 414);

finishing necessary circuit operations within said selected circuit blocks (112, 114, 412, 414) prior to shutting down said selected circuit blocks; and

shutting down said selected circuit blocks.

9. A method of powering down individual circuit blocks according to Claim 8, characterized in that said method further comprises generating a signal (144) that said selected circuit blocks have shutdown after said selected circuit blocks have shutdown.

10. A method of powering down individual circuit blocks according to Claim 9, characterized in that it further comprises preventing said system clock (130) from acting as said local clock (310) in said selected circuit blocks after said signal that selected circuit blocks have shutdown (144) is generated.

11. A method of powering down individual circuit blocks according to Claim 10 characterized in that preventing said system clock (130) from acting as said local clock (310) comprises disconnecting said system clock (130) from said local clock (310) only when said signal to power down (142) selected circuit blocks and said signal that selected circuit blocks have shutdown (144) is received at a logic circuit (300).